HFinFET: A Scalable, High Performance, Low Leakage Hybrid N-Channel FET

Kausik Majumdar, Prashant Majhi, Navakanta Bhat and Raj Jammy

***Abstract*—In this letter we propose the design and simulation study of a novel transistor, called HFinFET, which is a hybrid of a HEMT and a FinFET, to obtain excellent performance and good off state control. Followed by the description of the design, 3D device simulation has been performed to predict the characteristics of the device. The device has been benchmarked against published state of the art HEMT as well as planar and non-planar Si NMOSFET data of comparable gate length using standard benchmarking techniques.**

***Index Terms*—FinFET, HEMT, Transistor Scaling, Coupled Poisson-Schrodinger Equations.**

I. Introduction

Due to scalability issues of bulk MOSFET, beyond 22nm technology node, it is necessary to look for alternative options to drive the semiconductor industry. FinFET is one of the proposed candidates which shows excellent subthreshold slope and hence scalability due to its nonplanar multi-gate structure [1], [2], [3]. On the other hand, HEMT devices [4], [5] and some variants of it [6] drive the performance of ultra-fast devices using III-V channel material. However, their off state control, gate leakage and scalability need to be addressed before using them in VLSI logic circuit applications. Hence the bulk planar MOSFET still remains the major technology driver in semiconductor industry.

The aim of this work is to come up with a novel solution that takes care of both high performance and low leakage, but staying in the quasi-MOS regime which makes it possible to fabricate the device without extensive deviation from the existing technology. In the rest of the paper, we propose a scalable hybrid device, called HFinFET, to meet such requirements, namely providing high ON state current using bulk conduction arising from HEMT-like mechanism, and good off-state control by FinFET-like mechanism. Followed by the description of the device in sec. II, we discuss the characteristics of the device in sec. III. The four benchmarking techniques proposed in [7], namely (1) intrinsic gate delay (τ) vs gate length (L_g), (2) subthreshold slope (SS) vs L_g, (3) Energy-delay product ($E.\tau$) vs L_g and (4) I_{on}/I_{off} vs τ are used to evaluate the performance of the device. The simulated results are benchmarked against published state of the art HEMT devices [4], [5] and planar/nonplanar MOS devices [3], [7], [8]. The proposed device shows good promise as one of the candidates to replace existing MOS technology in the future.

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II. Transistor Design and Simulation

The top view of the proposed device is shown in Fig. 1(a). The corresponding cross section along AA′ is captured in Fig. 1(b). The architecture resembles a FinFET with two vertical

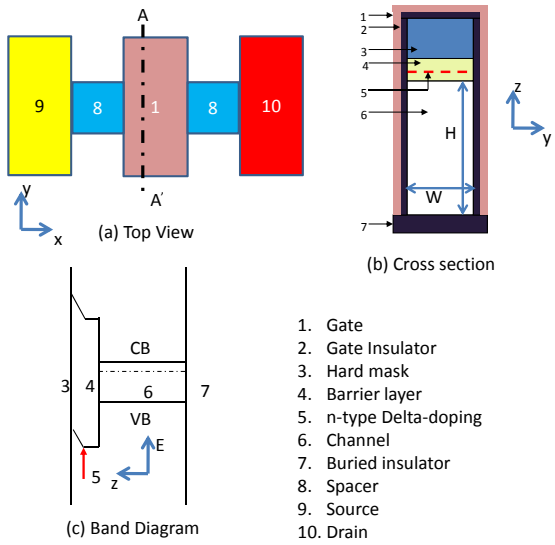

Fig. 1. The (a) top view, (b) cross-section and (c) schematic band diagram in the z direction of the proposed device HFinFET.

gates on the sides of the rectangular $In_{0.53}Ga_{0.47}As$ fin of width W and height H sitting on top of a burried insulator. However, instead of the hard mask directly sitting on top of the channel, a barrier layer is sandwiched between the channel and the hard mask. The barrier layer is selected such that it has a conduction band edge offset with the channel. Also, the barrier layer is almost lattice matched with the channel material so as to minimize the traps at its interface with the channel. The hard mask can be thick enough to make the channel immune to the top gate to reduce so called corner effects. The schematic band diagram in the vertical z direction is shown in Fig. 1(c). An n-type delta doped layer in the barrier layer can supply electrons in the channel at ON state, like a HEMT operation. Using a mid-gap workfunction gate material with no gate bias and n-doped source and drain,

the device conducts current, similar to a HEMT, providing excellent ON characteristics due to bulk conduction. We also note that the small geometrical cross section of the fin and the wavefunction pushing effect from the surface due to the low effective mass of $In_{0.53}Ga_{0.47}As$ help to achieve volume inversion, causing a spread of carrier distribution all along the cross section of the fin. Clearly, there is a distinction of turning ON mechanism between the proposed device and *'MOS-like'* devices including FinFET. The proposed device does not require any gate induced surface inversion. This helps the transistor to operate at very low electric field in the yz plane achieving much lower carrier scattering rate. However, unlike HEMT and more like a FinFET, the device is turned off by applying negative bias at the side gates, thus achieving excellent gate control providing good off state characteristics.

The device, as described in Fig. 1, is operating in depletion mode where we need to switch off the 'normally ON' transistor by applying negative bias at the gates. This depletion mode transistor can be converted into an enhancement mode by using gate workfunction engineering [4], [5]. In the rest of the paper, we assume a gate workfuntion such that the flatband voltage is V_{dd}. It should be noted that this workfunction engineering does not impact the low vertical field during ON state, but helps to shift the threshold voltage of the device from negative to positive. This flatband ON condition [9], coupled with the bulk conduction mechanism and inherently large mean free path of $In_{0.53}Ga_{0.47}As$ helps to operate the transistor very close to the ballistic limit.

An effective mass (m^*) based 3D self-consistent Poisson-Schrodinger solver coupled with ballistic transport model has been developed to simulate the device. Instead of bulk effective mass, we use a fin width dependent in-plane and quantization effective mass as shown in Fig. 2(a). Since the fin height is comparatively large, the effective mass is assumed to depend only on fin width. The in-plane effective mass m^*_{zx} of $In_{0.53}Ga_{0.47}As$ fin is extracted by separately fitting a parabola at the conduction band minimum of the bandstructure (obtained from a $sp^3d^5s^*$ tight-binding method [10]) of a thin film of InAs and GaAs followed by subsequent interpolation using Vegard law [11]. The quantization mass m^*_y is extracted by finding the energy difference of the conduction band minimum between the bulk and the thin film followed by similar interpolation. We also note that due to strong quantization and low voltage operation, the satellite valley spill over effect is negligible in thin $In_{0.53}Ga_{0.47}As$ channel and hence all the carriers can be safely assumed to be in the Γ valley [12]. The ballistic transport model is one similar to the model in [13] and does not take into account the tunneling components of the drain current. We analyze three different devices with L_g as 20nm, 15nm and 10nm. The doping density of the delta doped layer is assumed to be 2×10^{12} cm^{-2}. A gate insulator EOT of 1nm, fin height(H) of 15nm and a gate to source/drain underlap of 5 nm are assumed for all the transistors. The hard mask thickness is assumed to be large enough so that the top gate does not have any effect on the transistor electrostatics. The fin widths (W) of different gate length devices are varied as 5nm, 7.5nm and 10nm. The supply voltage has been taken to be 0.5V.

III. Results and Performance Evaluation

Fig. 2(b) and (c) show typical output and transfer characteristics of the device with L_g=20nm and W=10nm. We note the excellent drain current saturation in Fig. 2(b) as compared to HEMT devices ([4], [5]). This, we believe, is arising because the proposed device has significantly lower EOT and double gate structure and thus has a much better gate control over the channel. For a given V_g, at relatively large drain bias, the sensitivity of the height of the source-channel barrier on the drain voltage is much less resulting in improved drain current saturation. To evaluate the realistic

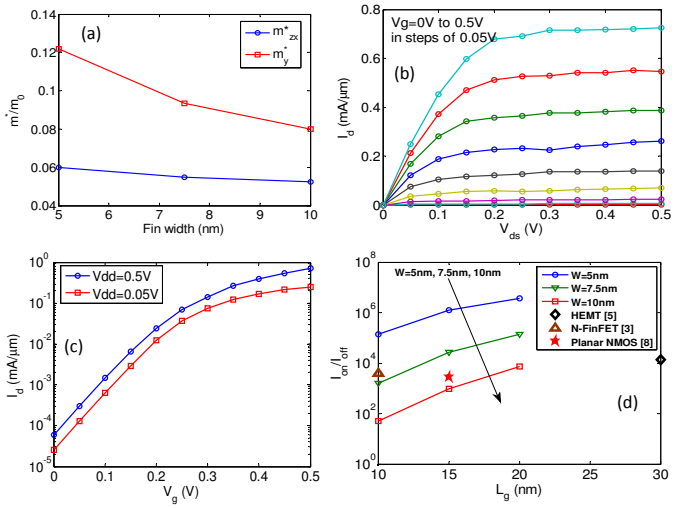

Fig. 2. (a): The in-plane (m^*_{zx}) and quantization effective mass (m^*_y) of $In_{0.53}Ga_{0.47}As$ extracted from $sp^3d^5s^*$ tight binding method using Vegard law. Both of them decrease with increase in fin width. (b): Simulated I_d-V_{ds} characteristics of HFinFET for fin width of 10nm and L_g=20nm shows excellent drain current saturation. (c): I_d-V_g characteristics of HFinFET for fin width of 10nm and L_g=20nm. (d): I_{on}/I_{off} ratio of HFinFET with Vdd=0.5V for different Fin widths, R_s=R_d=200Ω-μm, compared against published HEMT, FinFET and Planar NMOS data.

ON state performance of the device, we assume source and drain series resistance R_s=R_d=200Ω-μm and their effects on transistor characteristics are taken into account as a posteriori effect as explained in [14]. Fig. 2(d) plots the I_{on}/I_{off} as a function of L_g for different W. Stronger quantization at lower fin width reduces the OFF state leakage significantly and hence we observe improvement in I_{on}/I_{off} when we reduce the fin width. The I_{on}/I_{off} ratio of a 30nm gate length InAs HEMT, obtained in [5] is plotted in the same figure for comparison. Also, results for a 10nm gate length Si FinFET [3] and 15nm gate length planar NMOSFET [8] are compared in the same plot.

The proposed HFinFET has very impressive DIBL characteristics as shown in Fig. 3(a) For comparison, the DIBL values for published HEMT [5], FinFET [3] and planar NMOS [7] are also shown in the same plot. It is evident that HFinFET has excellent short channel behavior. As a part of the benchmarking study of the device using the four performance criteria described in [7], we have plotted the subthreshold slope numbers, obtained from the simulation, in Fig. 3(b) and compared against different state of the art devices. Fig. 4(a)

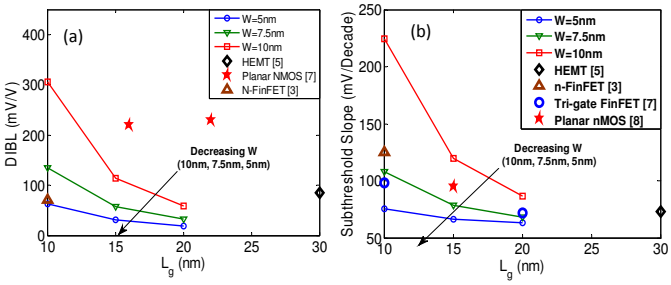

Fig. 3. (a) DIBL and (b) Subthreshold slope characteristics of HFinFET, compared against published HEMT, FinFET and Planar NMOS data.

shows the intrinsic gate delay as a function of L_g for different fin widths. As expected, stronger quantization arising from lower fin width degrades the ON current and hence gate delay. The intrinsic gate delays obtained compare very well with published high performance HEMT as well as planar and non-planar Si nMOSFETs, at different gate lengths. Note that, at L_g=10nm, the HFinFET with W=7.5nm and W=10nm meets the intrinsic gate delay projection of 0.167ps by ITRS 2007, however W=5nm misses the target. It is worthy to mention here that at smaller fin width, due to quantization, the gate capacitance also reduces slightly, which actually compensates for the delay degradation to some extent. Hence the ON current degradation is not completely reflected in delay degradation. The switching of less charge due to quantization impacts the energy-delay product of the device, which is shown in Fig. 4(b) and compared against planar NMOSFET data from [8]. Lower energy-delay product of the transistor makes it suitable for low power and high performance logic circuits. Finally, the simulated data points are plotted in the delay

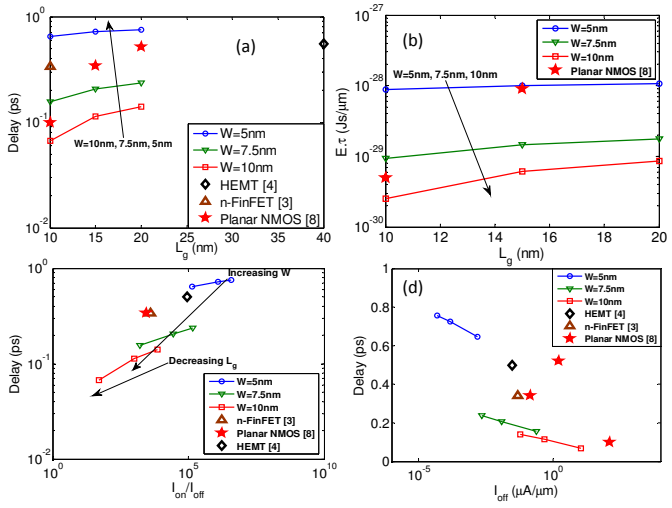

Fig. 4. (a) Intrinsic gate delay (CV/I) and (b) Energy-delay product ($E.\tau$) of HFinFET with Vdd=0.5V and R_s=R_d=200Ω-μm. Comparison of relative performance of HFinFET, HEMT, FinFET and Planar NMOS in the (c) Delay versus I_{on}/I_{off} design space and (d) Delay versus I_{off} design space. The relatively higher delay of the HEMT device is due to the larger channel length (40nm) of the device.

versus I_{on}/I_{off} design space in Fig. 4(c) which shows that narrower fin widths provide better ON to OFF current ratio, but reducing the fin width too much kills the intrinsic gate delay. When the results are compared against reported state of the art devices, HFinFET is found to shift the operating points towards the ideal right bottom corner of the design space. To further probe the claim of better performance as well as lower OFF state current in HFinFET, we have shown the device performance in the delay versus I_{off} space in Fig. 4(d). Compared to existing devices, The proposed device shows significantly improved intrinsic gate delay at a given OFF state leakage showing the potential to actually provide high performance like HEMT/bulk nMOSFET and at the same time good off state control like a FinFET.

IV. Conclusion

To conclude, in this letter, we have presented the design and systematic simulation of a novel hybrid $In_{0.53}Ga_{0.47}As$ n channel transistor, called HFinFET, which uses the best of both the worlds of a HEMT and a FinFET, i.e. high performance and good off state control. The simulations results have been benchmarked using standard device performance criteria and compared with available state of the art devices including HEMT, bulk planar NMOS and n-FinFET. Further investigation is required to optimize the different device parameters. However, the preliminary study reveals that an optimized HFinFET has the potential to be a promising candidate for the next generation transistor to help continue scaling.

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